



USER MANUAL

Adrastea-I 2615011136000

VERSION 1.1

May 26, 2023

WURTH ELEKTRONIK MORE THAN YOU EXPECT

MUST READ

Check for firmware updates

Before using the product make sure you use the most recent firmware version, data sheet and user manual. This is especially important for Wireless Connectivity products that were not purchased directly from Würth Elektronik eiSos. A firmware update on these respective products may be required.

We strongly recommend to include in the customer system design, the possibility for a firmware update of the product.

Certification Information:

The certification information is mandatory to check, see chapter 1.3



Revision history

Manual version	FW version	HW version	Notes	Date
1.0	ADRASTEA- I_06.006	1.0	 Initial release of the manual 	April 2022
1.1	ADRASTEA- I_06.006	1.0	 Added section Adrastea-I GCF Certification. Added section Minimal pin connections. Updated section Application MCU Software Development Kit. 	May 2023



Abbreviations

Abbreviation	Name
3GPP	3rd Generation Partnership Project
ADC	Analog-to-Digital Converter
ASCI	Advanced Speech Call Items
APN	Access Point Name
BCD	Binary Coded Decimal
DH	Deep Hibernation
EJTAG	Embedded Joint Test Action Group
GLONASS	Global Navigation Satellite System
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
GPIO	General Purpose Input Output
l ² C	Inter-Integrated Circuit
IoT	Internet of Things
IMEI	International Mobile station Equipment Identity
IMEISV	International Mobile station Equipment Identity and Software Version number
JTAG	Joint Test Action Group
LTE	Long Term Evolution
MCU	Micro controller Unit
MSIO	Master In Slave Out
ME	Mobile Equipment
MT	Mobile Termination
MTU	Maximum Transfer Unit
PA	Power Amplifier
PD	Power Down
PMU	Power Management Unit
PSM	Power Save Mode
RAM	Random Access Memory
RLP	Radio Link Protocol
RTC	Real Time Clock
SINAD	Signal to Noise and Distortion ratio
SIM	Subscriber Identity Module
SPI	Serial Peripheral Interface
SVN	Software Version Number



ТА	Terminal Adaptor
тсхо	Temperature Compensated Crystal Oscillator
TE	Terminal Equipment
TTFF	Time To First Fix
UART	Universal Asynchronous Receiver/Transmitter
UE	User Equipment
UICC	Universal Integrated Circuit Card
USIM	Universal Subscriber Identity Module
ХО	Crystal Oscillator



Contents

1	Introd 1.1 1.2 1.3 1.4 1.5 1.6 1.7	Adrastea-I GCF Certification9Adrastea-I Deutsche Telekom Certification10Benefits of Deutsche Telekom Certified Module11Connectivity13Module Key Features14Block diagram15Ordering information15	3 3 1 3 4 5 5
2	Electr	rical and Radio Specifications 16	5
	2.1	Recommended Operating Conditions	3
	2.2	Current Consumption	3
		2.2.1 LTE-Cat.M Mode	3
		2.2.2 LTE-Cat.NB-IoT Mode	7
	2.3	LTE Radio Characteristics	7
		2.3.1 LTE Supported Bands	3
			3
			3
		2.3.4 RF Receiving Sensitivity	1 \
		2.3.5 LTE-Cal.M Reference sensitivity 10	י ג
		2.3.7 Maximum Output Power 20	,)
		2.3.8 LTE-Cat.M Maximum Output Power	ý
		2.3.9 LTE-Cat.NB-IoT Maximum Output Power)
	2.4	GNSS Radio Characteristics)
		2.4.1 GNSS Supported Constellation	I
		2.4.2 GNSS: Operating frequencies	I
		2.4.3 GNSS: Rx Sensitivity	l
		2.4.4 GNSS: Time To First Fix	2
		2.4.5 GNSS: Position Accuracy	2
z	Pinou	t og	z
Ū	3.1	Module Power Up	ŝ
	3.2	Module Power Down	9
	3.3	Module Reset	9
	3.4	WAKEUP pin)
	3.5	AT_IN and AT_OUT pins)
	3.6	/RESET pin)
	3.7	EXT_ALARM pin	I
	3.8	RF_LTE pin	1
	3.9	RF_GNSS pin	
	3.10		ן ר
			2 2
		3.10.2 VDAURUF PIII	- >
	3 1 1	F-ITAG Debug port	- २
	0.11		1

User manual Adrastea-I



	3.12 3.13	GPIO Pin Information	34 34			
4 Module Interfaces						
-	/ 1		35			
	4.1		22			
			30			
			30			
			36			
		4.1.4 UART2 Pin Interface	37			
		4.1.5 UART0 Host Connection	37			
	4.2	SPI Interface	39			
		4.2.1 SPIM Pin Interface	39			
		4.2.2 SPIM Connection	39			
	43	I ² C Interface	41			
	1.0	4.3.1 l^2 C. Pin Interface	<u>4</u> 1			
		$4.3.2$ I^2 C Connection	<u>/1</u>			
	1 1		41			
	4.4		43			
			43			
			44			
	4.5	SIM Interface	44			
		4.5.1 SIM Pin Interface	44			
	4.6	RF interfaces	45			
	4.7	E-JTAG Debug port	45			
	4.8	GPIO Pin Information	46			
5	Funct	tional description	47			
5	Func 5 1	t ional description Adrastea-I State Transition	47 47			
5	Func 5.1	tional description Adrastea-I State Transition	47 47 ∕18			
5	Func 5.1 5.2	tional description Adrastea-I State Transition Adrastea-I Power Saving Modes 5.2.1 DH0 Mode	47 47 48 48			
5	Func 5.1 5.2	tional description Adrastea-I State Transition Adrastea-I Power Saving Modes 5.2.1 DH0 Mode 5.2.2	47 47 48 48			
5	Funct 5.1 5.2	tional description Adrastea-I State Transition Adrastea-I Power Saving Modes 5.2.1 DH0 Mode 5.2.2 DH1 Mode	47 48 48 48 48			
5	Func 5.1 5.2	tional description Adrastea-I State Transition Adrastea-I Power Saving Modes 5.2.1 DH0 Mode 5.2.2 DH1 Mode 5.2.3 DH2 Mode	47 48 48 48 48 49			
5	Func 5.1 5.2 5.3	tional description Adrastea-I State Transition	47 48 48 48 49 49			
5	Func 5.1 5.2 5.3	tional descriptionAdrastea-I State TransitionAdrastea-I Power Saving Modes5.2.1DH0 Mode5.2.2DH1 Mode5.2.3DH2 ModeGNSS Receiver5.3.1Supported GNSS constellations	47 48 48 48 49 49 49			
5	Func 5.1 5.2 5.3	tional descriptionAdrastea-I State TransitionAdrastea-I Power Saving Modes5.2.1 DH0 Mode5.2.2 DH1 Mode5.2.3 DH2 ModeGNSS Receiver5.3.1 Supported GNSS constellations5.3.2 GNSS Co-existence with LTE Modem	47 48 48 49 49 49 49			
5	Func 5.1 5.2 5.3 5.4	tional description Adrastea-I State Transition	47 48 48 49 49 49 49 50			
5	Func 5.1 5.2 5.3 5.4	Adrastea-I State TransitionAdrastea-I Power Saving Modes5.2.1 DH0 Mode5.2.2 DH1 Mode5.2.3 DH2 Mode5.3.1 Supported GNSS constellations5.3.2 GNSS Co-existence with LTE Modem5.4.1 Application MCU5.4.1 Application MCU Software Development Kit	47 48 48 49 49 49 49 50 50			
5	Func 5.1 5.2 5.3 5.4 Quick	tional description Adrastea-I State Transition Adrastea-I Power Saving Modes 5.2.1 DH0 Mode 5.2.2 DH1 Mode 5.2.3 DH2 Mode 5.2.3 DH2 Mode GNSS Receiver 5.3.1 Supported GNSS constellations 5.3.2 GNSS Co-existence with LTE Modem Application MCU 5.4.1 Application MCU Software Development Kit	47 48 48 49 49 49 50 50 50 53			
6	Func 5.1 5.2 5.3 5.4 Quick 6.1	tional description Adrastea-I State Transition Adrastea-I Power Saving Modes 5.2.1 DH0 Mode 5.2.2 DH1 Mode 5.2.3 DH2 Mode 5.2.3 DH2 Mode GNSS Receiver 5.3.1 Supported GNSS constellations 5.3.2 GNSS Co-existence with LTE Modem Application MCU 5.4.1 Application MCU Software Development Kit Start guide Minimal pin connections	47 48 48 49 49 49 50 50 53			
5	Func 5.1 5.2 5.3 5.4 Quick 6.1 6.2	tional description Adrastea-I State Transition Adrastea-I Power Saving Modes 5.2.1 DH0 Mode 5.2.2 DH1 Mode 5.2.3 DH2 Mode GNSS Receiver 5.3.1 Supported GNSS constellations 5.3.2 GNSS Co-existence with LTE Modem Application MCU 5.4.1 Application MCU Software Development Kit Start guide Minimal pin connections Prerequisities	47 47 48 48 49 49 49 50 50 53 53 54			
5	Func 5.1 5.2 5.3 5.4 Quick 6.1 6.2	tional description Adrastea-I State Transition Adrastea-I Power Saving Modes 5.2.1 DH0 Mode 5.2.2 DH1 Mode 5.2.3 DH2 Mode GNSS Receiver 5.3.1 Supported GNSS constellations 5.3.2 GNSS Co-existence with LTE Modem Application MCU 5.4.1 Application MCU Software Development Kit Start guide Minimal pin connections Prerequisites Taking into appartice	47 48 48 49 49 49 50 50 53 53 54 56			
5 6	Funct 5.1 5.2 5.3 5.4 Quick 6.1 6.2 6.3 0.4	tional description Adrastea-I State Transition Adrastea-I Power Saving Modes 5.2.1 DH0 Mode 5.2.2 DH1 Mode 5.2.3 DH2 Mode GNSS Receiver 5.3.1 Supported GNSS constellations 5.3.2 GNSS Co-existence with LTE Modem Application MCU 5.4.1 Application MCU Software Development Kit Start guide Minimal pin connections Prerequisites Taking into operation Calast I TE Mode	47 48 48 49 49 49 50 50 53 53 54 56			
6	Func 5.1 5.2 5.3 5.4 Quick 6.1 6.2 6.3 6.4	tional description Adrastea-I State Transition Adrastea-I Power Saving Modes 5.2.1 DH0 Mode 5.2.2 DH1 Mode 5.2.3 DH2 Mode GNSS Receiver 5.3.1 Supported GNSS constellations 5.3.2 GNSS Co-existence with LTE Modem Application MCU 5.4.1 Application MCU Software Development Kit 5.4.1 Application MCU Software Development Kit Start guide Minimal pin connections Prerequisites Taking into operation Select LTE-M or NB-IoT Mode	47 48 48 49 49 49 50 50 53 53 54 56 59			
6	Funct 5.1 5.2 5.3 5.4 Quick 6.1 6.2 6.3 6.4 6.5	tional description Adrastea-I State Transition Adrastea-I Power Saving Modes 5.2.1 DH0 Mode 5.2.2 DH1 Mode 5.2.3 DH2 Mode GNSS Receiver	47 48 48 48 49 49 49 50 50 53 53 54 56 59 60			
6	Func 5.1 5.2 5.3 5.4 Quick 6.1 6.2 6.3 6.4 6.5 6.6	tional description Adrastea-I State Transition Adrastea-I Power Saving Modes 5.2.1 DH0 Mode 5.2.2 DH1 Mode 5.2.3 DH2 Mode GNSS Receiver 5.3.1 Supported GNSS constellations 5.3.2 GNSS Co-existence with LTE Modem Application MCU 5.4.1 Application MCU Software Development Kit 5.4.1 Application MCU Software Development Kit Start guide Minimal pin connections Prerequisites Taking into operation Select LTE-M or NB-IoT Mode Register to Network Activate GNSS	47 48 48 49 49 49 50 50 53 53 54 56 50 61			
5 6 7	Funct 5.1 5.2 5.3 5.4 Quick 6.1 6.2 6.3 6.4 6.5 6.6 Desic	tional description Adrastea-I State Transition Adrastea-I Power Saving Modes 5.2.1 DH0 Mode 5.2.2 DH1 Mode 5.2.3 DH2 Mode GNSS Receiver 5.3.1 Supported GNSS constellations 5.3.2 GNSS Co-existence with LTE Modem Application MCU 5.4.1 Application MCU Software Development Kit 5.4.1 Application MCU Software Development Kit Start guide Minimal pin connections Prerequisites Taking into operation Select LTE-M or NB-IoT Mode Register to Network Activate GNSS	47 48 48 49 49 50 50 53 53 54 56 60 61 64			
5 6 7	Funct 5.1 5.2 5.3 5.4 Quick 6.1 6.2 6.3 6.4 6.5 6.6 Desig 7.1	tional description Adrastea-I State Transition Adrastea-I Power Saving Modes 5.2.1 DH0 Mode 5.2.2 DH1 Mode 5.2.3 DH2 Mode GNSS Receiver 5.3.1 Supported GNSS constellations 5.3.2 GNSS Co-existence with LTE Modem Application MCU 5.4.1 Application MCU Software Development Kit 5.4.1 Application MCU Software Development Kit start guide Minimal pin connections Prerequisites Taking into operation Select LTE-M or NB-IoT Mode Register to Network Activate GNSS	47 48 48 49 49 49 50 50 53 53 54 56 50 61 64 64			
5 6 7	Funct 5.1 5.2 5.3 5.4 Quick 6.1 6.2 6.3 6.4 6.5 6.6 Desig 7.1 7.2	tional description Adrastea-I State Transition Adrastea-I Power Saving Modes 5.2.1 DH0 Mode 5.2.2 DH1 Mode 5.2.3 DH2 Mode GNSS Receiver 5.3.1 Supported GNSS constellations 5.3.2 GNSS Co-existence with LTE Modem Application MCU 5.4.1 Application MCU Software Development Kit start guide Minimal pin connections Prerequisites Taking into operation Select LTE-M or NB-IoT Mode Register to Network Activate GNSS	47 48 48 49 49 49 50 53 53 56 56 61 64 66 66			

User manual Adrastea-I



	7.3	Antenna solutions 6 7.3.1 Wire antenna 6 7.3.2 Chip antenna 6 7.3.3 PCB antenna 6	6 7 7
8	Refer 8.1 8.2	ence design Schematic	8 9 4
9	Manu 9.1 9.2 9.3 9.4	facturing information7Moisture sensitivity level7Soldering79.2.1Reflow soldering79.2.2Cleaning79.2.3Potting and coating79.2.4Other notations7ESD handling7Safety recommendations7	6 6 6 8 8 8 9 9
10	Physi 10.1 10.2 10.3 10.4	cal specifications8Dimensions8Weight8Module drawing8Footprint8	1 1 1 2 3
11	Marki 11.1 11.2	ng Lot number	4 5
12	Refere	ences 8	6
13	Regul 13.1 13.2 13.3 13.4	atory compliance information8Important notice EU8Conformity assessment of the final product8Exemption clause8EU Declaration of conformity8	7 777 787
14	Impor 14.1 14.2	tant notes 8 General customer responsibility 8 Customer responsibility related to specific, in particular safety-relevant appli-	9
	14.3 14.4 14.5 14.6 14.7 14.8	cations8Best care and attention8Customer support for product specifications8Product improvements9Product life cycle9Property rights9General terms and conditions9	9 9 9 0 0 0

User manual Adrastea-I



15	Legal 15.1 15.2 15.3 15.4	noticeExclusion of liabilitySuitability in customer applicationsTrademarksUsage restriction	91 91 91 91 91
16	Licen	se terms	93
	16.1	Limited license	93
	16.2	Usage and obligations	93
	16.3	Ownership	94
	16.4	Firmware update(s)	94
	16.5	Disclaimer of warranty	94
	16.6	Limitation of liability	95
	16.7	Applicable law and jurisdiction	95
	16.8	Severability clause	95
	16.9	Miscellaneous	95



1 Introduction

Adrastea-I module is a compact LTE-M/NB-IoT Cellular module with integrated GNSS, integrated ARM Cortex-M4 and 1MB Flash memory for customer developed applications.

Based on the Sony Altair ALT1250 chipset, the Adrastea-I module provides AT-Command based multi-band configurability enabling international multi-regional coverage in LTE Cat M1 / NB1 radio access technologies.

Adrastea-I includes a fully integrated global navigation satellite system solution that supports GPS and GLONASS positioning systems.

The ARM Cortex-M4 processor is exclusively for user application software, and it offers 1 MB of flash and 256 kB of RAM dedicated to this use.

Compact 13.4mm x14.6mm x 1.85mm design allows the module to fit in small-size applications.

The module can be operated through one of two available cellular communication technologies:

- LTE-Cat.M or
- LTE-Cat.NB-IoT.

The Adrastea-I evaluation kit and "Adrastea Commander" tool ([1]) allow getting started with the module and testing its functionalities. The evaluation board can be connected to an USB port of a PC. The evaluation board also represents our reference design. For further information, please refer to the evaluation board manual [2].

The module comes with the declaration of conformity (CE), is compliant to RoHS, REACH. The Adrastea-I module is GCF and Deutsche Telekom certified.



Figure 1: Adrastea-I



1.1 Adrastea-I GCF Certification

Adrastea-I is GCF certified module. Major advantage with GCF certified module integrated in end IoT application is that it reduces efforts for industry and operator specific certifications. However, customer shall check certification requirements with network operator before commercial deployment of IoT devices.



Figure 2: Adrastea-I GCF Certification



1.2 Adrastea-I Deutsche Telekom Certification

Adrastea-I is certified by Deutsche Telekom.



Figure 3: Adrastea-I Deutsche Telekom Certification



1.3 Benefits of Deutsche Telekom Certified Module

Normal Cellular Cerfication procedure includes 3 different types of certifications:

- Regulatory Certification: CE, FCC and similar based on region.
- Industry Specific Certification: GCF, PTCRB
- Network Operator Certification: Vodafone, Deutsche Telekom, AT&T etc.



* To do on device level, Adrastea-I offers CE declaration

** To do on device level, Adrastea-I offers GCF certification

Figure 4: Normal Cellular Certification Process

Pre-Certified Adrastea-I module from Deutsche Telekom brings the following key advantages:

• It enables integration to end device without further end device label Industry specific Certification (i.e. GCF) and Network Operator Certification (Deutsche Telekom).





Regulatory Certifications (i.e. CE, FCC and similar based on region) are still required for the end product.

- Obtain assurance: Pre-certified module reduces the final test effort.
- Save time and money: The end product does not require to go through complex cellular certification process again.



Benefits of certification are applicable only when customer uses connectivity (IoT SIM cards) from Deutsche Telekom. To get the certification benefit, the customer must use connectivity (IoT SIM cards) from Deutsche Telekom



*To do on device level, Adrastea-I offers CE declaration
 Figure 5: Benefits of Deutsche Telekom Certified Module



1.4 Connectivity

IoT SIM cards can be ordered from WE-DTAG Connectivity Portal *https://iotcreators.com/wuerth/*.

Strong partnership of Würth Elektronik eiSos and Deutsche Telekom offers many advantages for message based connectivity:

- End device label certification Industry specific Certification and Network Operator Certification is not required. Regulatory Certifications (i.e. CE, FCC and similar based on region) is still required for the end product.
- Technology independent charges.
- Roaming charges included. This enables devices to connect on roaming partners networks where Deutsche Telekom does not have network coverage.
- Option for standard and Industrial 2FF/3FF/4FF/MFF2 SIMS.
- Easy online ordering and easy payment.
- Stay flexible and grow at your own speed. As of today one free IoT SIM (i.e. "Starterkit") can be ordered via the portal for testing purposes.
- NB-IoT and LTE-M coverage map is designed to check LTE-M and NB-IoT in different countries.
- Message-brokerage service with NB-IoT / LTE-M connectivity. As of today 120 messages per SIM per day are allowed.



1.5 Module Key Features

Feature	Description
Physical Dimensions	13.4mm x 14.6mm x 1.85mm
Supported Networks	- LTE-Cat.M - LTE-Cat.NB-IoT
LTE Supported Bands	LTE-Cat.M: B2/B3/B4/B5/B8/B12/B20/B25/B26/B28 LTE-Cat.NB-IoT: B3/B5/B8/B20/B28
Module Interfaces	- USIM - UART - I ² C Master - SPI Master - GPIO - ADC - JTAG
Integrated GNSS	Adrastea-I includes a fully integrated global navigation satellite system solution that supports GPS and GLONASS positioning system.
Integrated User MCU	User MCU is exclusively for user application software: - ARM Cortex-M4 - 1 MB Flash Memory - 256 kB RAM
Output Power class	Power Class 3 (23 dBm)
Maximum Data Rate	LTE-Cat.M: Downlink: 300 Kbps, Uplink: 375 Kbps
	LTE-Cat.NB-IoT: Downlink: 27.2 Kbps, Uplink: 62.5 Kbps
3GPP Standard Compliance	3GPP Release 13 compliant, Upgradable to Rel 14
Firmware Upgrade	 Firmware upgrade over USB interface Firmware upgrade over air
Supported Protocols	- IPv4, IPv6 - TPC/UDP SOCKET - HTTP/HTTPS - TLS/DTLS - LWM2M Client - MQTT
AT Commands	3GPP TS 27.007 and 3GPP TS 27.005 AT commands, as well as Würth Elektronik eiSos enhanced AT commands
Operating Voltage	- VDD: From 2.3 V to 4.3 V - VDD_FEM: From 3.1 V to 4.3 V
Temperature Range	Operation temperature: -40 ℃ to +85 ℃

Table	1:	Module	Key	Features
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1.6 Block diagram





1.7 Ordering information

WE order code	Description
2615011136000	Cellular LTE-M/NB-IoT module in T&R packaging
2615029236001	Cellular LTE-M/NB-IoT EV-Kit

Table 2: Ordering information



2 Electrical and Radio Specifications

Unless otherwise stated, all the values given in the manual were measured on the Adrastea-I evaluation board under the following conditions: $T = 25 \,^{\circ}$ C and powered via 5 V/1A Power Jack. The voltage regulator of the EV board regulates the connected voltage 5 V down to 3.6 V and supplies the remaining parts of the circuit. If the evaluation board is power sourced, the power LED1 lights up.

2.1 Recommended Operating Conditions

Parameter	Direction	Min.	Тур.	Max.	Unit
Supply voltage (VDD)	Supply	2.3	3.6	4.3	V
Supply voltage (VDD_FEM)	Supply	3.1	3.6	4.3	V
VSIM	Output	1.7	1.8	1.9	V
VDDIO	Output	1.7	1.8	1.9	V
Operating temperature		-40	25	85	°C

Table 3: Recommended operating conditions

2.2 Current Consumption

2.2.1 LTE-Cat.M Mode

Description	Test Condition	Value	Unit
LTE-IDLE	MCU RUN	16.8	mA
	MCU SHUTDOWN	2.9	mA
Peak Current (TX)	TX @23dBm, MCU RUN	454.2	mA
PSM Current (DH0)	MCU SHUTDOWN, LTE RF Disabled (AT+CFUN=0)	1.57	μA
PSM Current (DH1)	MCU SHUTDOWN, LTE RF Disabled (AT+CFUN=0)	39.6	μA
PSM Current (DH2)	MCU SHUTDOWN, LTE RF Disabled (AT+CFUN=0)	82.2	μA
GNSS-Active	MCU RUN, LTE RF Disabled (AT+CFUN=0)	53.98	mA

Table 4: LTE-Cat.M Current consumption



2.2.2 LTE-Cat.NB-IoT Mode

Description	Test Condition	Value	Unit
LTE-IDLE	MCU RUN	15.7	mA
	MCU SHUTDOWN	2.8	mA
Peak Current (TX)	TX @23dBm, MCU RUN	434	mA
PSM Current (DH0)	MCU SHUTDOWN, LTE RF Disabled (AT+CFUN=0)	1.57	μA
PSM Current (DH1)	MCU SHUTDOWN, LTE RF Disabled (AT+CFUN=0)	38.5	μA
PSM Current (DH2)	MCU SHUTDOWN, LTE RF Disabled (AT+CFUN=0)	81.5	μA

Table 5: NB-IoT Current consumption

2.3 LTE Radio Characteristics

Module performance is based on the quality of the RF link from LTE network to the Adrastea-I module.

The following factors and tasks are critical for the performance of the Adrastea-I module:

- External LTE antenna for signal reception from LTE network.
- RF trace delivering the signal from the external antenna to the LTE RF pad of the Adrastea-I module
- Minimization of external and environmental effects.



2.3.1 LTE Supported Bands

2.3.2 LTE-Cat.M Mode

Band	Transmit Band (Tx)	Receive Band (Rx)	Unit
B2	1850 - 1910	1930 - 1990	MHz
B3	1710 - 1785	1805 - 1880	MHz
B4	1710 - 1755	2110 - 2155	MHz
B5	824 - 849	869 - 894	MHz
B8	880 - 915	925 - 960	MHz
B12	699 - 716	729 - 746	MHz
B20	832 - 862	791 - 821	MHz
B25	1850 - 1915	1930 - 1995	MHz
B26	814 - 849	859 - 894	MHz
B28	703 - 748	758 - 803	MHz

Table 6: LTE-Cat.M Supported Bands

2.3.3 LTE-Cat.NB-IoT Mode

Band	Transmit Band (Tx)	Receive Band (Rx)	Unit
B3	1710 - 1785	1805 - 1880	MHz
B5	824 - 849	869 - 894	MHz
B8	880 - 915	925 - 960	MHz
B20	832 - 862	791 - 821	MHz
B28	703 - 748	758 - 803	MHz

Table 7: LTE-Cat.NB-IoT Supported Bands



2.3.4 RF Receiving Sensitivity

Unless noted otherwise, the Adrastea-I evaluation boad is in static mode, values were measured with Rohde and Schwarz CMW500 equipment.

2.3.5 LTE-Cat.M Reference sensitivity

Band	Band Width	Value	Unit
B2	1.4 MHz	-105	dBm
B3	1.4 MHz	-106.4	dBm
B4	1.4 MHz	-106.2	dBm
B5	1.4 MHz	-106.2	dBm
B8	1.4 MHz	-107.2	dBm
B12	1.4 MHz	-105.6	dBm
B20	1.4 MHz	-106.4	dBm
B25	1.4 MHz	-106.8	dBm
B26	1.4 MHz	-106.4	dBm
B28	1.4 MHz	-106	dBm

Table 8: LTE-Cat.M RX Sensitivity

2.3.6 LTE-Cat.NB-IoT Reference sensitivity

Band	Value	Unit
B3	-110	dBm
B5	-110	dBm
B8	-110	dBm
B20	-110	dBm
B28	-110	dBm

Table 9: LTE-Cat.NB-IoT RX Sensitivity



2.3.7 Maximum Output Power

Unless noted otherwise, the Adrastea-I evaluation boad is in static mode, values were measured with Rohde and Schwarz CMW500 equipment.

2.3.8 LTE-Cat.M Maximum Output Power

Band	Band Width	Value	Unit
B2	5 MHz	22.9	dBm
B3	5 MHz	21.5	dBm
B4	5 MHz	21.4	dBm
B5	5 MHz	21.7	dBm
B8	5 MHz	22.9	dBm
B12	5 MHz	21.4	dBm
B20	5 MHz	21.7	dBm
B25	5 MHz	23.0	dBm
B26	5 MHz	21.8	dBm
B28	5 MHz	21.9	dBm

Table 10: LTE-Cat.M Maximum Output Power

2.3.9 LTE-Cat.NB-IoT Maximum Output Power

Band	Value	Unit
B3	21.8	dBm
B5	22.0	dBm
B8	23.7	dBm
B20	22.1	dBm
B28	22.4	dBm

Table 11: LTE-Cat.NB-IoT Maximum Output Power

2.4 GNSS Radio Characteristics

Module performance is based on the quality of the RF link from GNSS satellites to the module.

The following factors and tasks are critical for the performance of the integrated GNSS:

• Free/unimpacted line of sight



- External GNSS antenna for signal reception from GNSS satellites
- RF trace delivering the signal from the external antenna to the RF pad of the GNSS module
- Minimization of external and environmental effects

Adrastea-I supports GPS and GLONASS satellite systems using dedicated hardware accelerators in a power and cost efficient manner. The GNSS receiver shares certain hardware resources with the modem. This enables GNSS measurement slots to be efficiently scheduled based on the modem link state. The device key target is to allow GNSS positioning for asset management applications where infrequent position updates are required.

The Adrastea-I GNSS shares the RF Rx path with the LTE modem and, therefore, cannot operate in parallel with LTE data transfer. Hence this GNSS is not suitable for products that inherently require this co-existence, LTE connection and GNSS tracking.



GNSS cannot co-exist with LTE data transfer. LTE communication has higher priority over GNSS and, therefore, GNSS is automatically shut down once LTE is active (if it was active). While LTE is active, GNSS cannot be activated and all GNSS AT commands are responded with error.

2.4.1 GNSS Supported Constellation

Adrastea-I supports the following constellation (Satellite systems):

- GPS
- GLONASS

2.4.2 GNSS: Operating frequencies

Description	Min	Тур.	Max	Unit
Input Frequency	1560		1610	MHz

Table 12: Radio characteristics

2.4.3 GNSS: Rx Sensitivity

Module sensitivity is the weakest signal level the receiver can work with and it depends on the state of the module.

• Cold start sensitivity is the minimum power required by the module to acquire satellites and perform first fix in cold start.



- Hot start sensitivity is the minimum power required by the module to acquire satellites and perform first fix in hot start.
- Tracking sensitivity is the minimum power required by the module to keep in track of the position fix.

Parameter	Test Condition	Value	Unit
Cold Start	GPS-GLONASS	-145	dBm
Hot Start	GPS-GLONASS	-152	dBm
Tracking	GPS-GLONASS	-160	dBm

Table 13: GNSS RX	Sensitivity
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2.4.4 GNSS: Time To First Fix

The Time To First Fix (TTFF) is the time needed by the module to achieve the first valid position fix, once the module is powered up or returns from a period of signal blockage.

Depending on the type of start (cold or hot), different TTFF performance is given below.

Parameter	Test Condition	Value	Unit
Cold Start	GPS-GLONASS, Power Level = -120dBm	36	S
Hot Start	GPS-GLONASS, Power Level = -120dBm	1	S

Table 14: GNSS Time to First Fix

2.4.5 GNSS: Position Accuracy

Parameter	Test Condition	Value	Unit
Position Accuracy	GPS-GLONASS, Power Level = -120dBm	1.5	m

Table 15: GNSS Position Accuracy



3 Pinout



Figure 7: Pinout (top view)



Pin Number	Designation	I/O	Description
1	GND	Supply	Negative Supply Voltage
2	GND	Supply	Negative Supply Voltage
3	VDD	Supply	Power supply for module
4	VDD	Supply	Power supply for module
5	VDD	Supply	Power supply for module
6	AT_IN	Input	Anti-tamper input
7	WAKEUP	Input	Wakeup active high
8	AT_OUT	Output	Anti-tamper output
9	/RESET	Input	Reset active low
10	EJ_TCK	Input	JTAG Test Clock
11	RESERVED	-	Reserved (Shall be soldered but not connected.)
12	EJ_TDO	Output	JTAG Test Data Output
13	EXT_ALARM	Output	Alarm Output
14	EJ_TDI	Input	JTAG Test Data Input
15	I2C0_SCL	Input/Output	I2C serial clock
16	EJ_TMS	Input	JTAG Test Mode Select
17	I2C0_SDA	Input/Output	I2C serial data
18	EJ_TRST	Input	JTAG Test Reset (required exter- nal pull down)
19	UART0_RTS	Output	MCU UART0 Request to Send
20	UART0_CTS	Input	MCU UART0 Clear to Send
21	UART0_TX	Output	MCU UART0 Transmit Data
22	UART0_RX	Input	MCU UART0 Receive Data
23	RESERVED	_	Reserved (Shall be soldered but not connected.)
24	RESERVED	_	Reserved (Shall be soldered but not connected.)

Table 16: Pinout

User manual Adrastea-I



Pin Number	Designation	I/O	Description		
25	VDD_FEM	Supply	Power supply for FEM (Front End Module)		
26	VDD_FEM	Supply	Power supply for FEM (Front End Module)		
27	VDD_FEM	Supply	Power supply for FEM (Front End Module)		
28	GND	Supply	Negative supply voltage		
29	GND	Supply	Negative supply voltage		
30	GND	Supply	Negative supply voltage		
31	GND	Supply	Negative supply voltage		
32	GND	Supply	Negative supply voltage		
33	GND	Supply	Negative supply voltage		
34	GND	Supply	Negative supply voltage		
35	GND	Supply	Negative supply voltage		
36	GND	Supply	Negative supply voltage		
37	GND	Supply	Negative supply voltage		
38	GND	Supply	Negative supply voltage		
39	RF_LTE	RF	RF Signal LTE		
40	GND	Supply	Negative supply voltage		
41	GND	Supply	Negative supply voltage		
42	GND	Supply	Negative supply voltage		
43	RF_GNSS	RF	RF Signal GNSS		
44	RESERVED	_	Reserved (Shall be sol- dered but not connected.)		
45	GND	Supply	Negative supply voltage		
46	GND	Supply	Negative supply voltage		
47	RESERVED	-	Reserved (Shall be sol- dered but not connected.)		
48	UART2_TX	Output	UART2 Transmit Data (CLI port)		
49	RESERVED	_	Reserved (Shall be sol- dered but not connected.)		
50	UART2_RX	Input	UART2 Receive Data (CLI port)		
51	GND	Supply	Negative supply voltage		
52	GND	Supply	Negative supply voltage		
53	UART2_CTS	Input	UART2 Clear to Send (CLI port)		

Table 17: Pinout1

User manual Adrastea-I



Pin Number	Designation	I/O	Description		
54	RESERVED	_	Reserved (Shall be sol- dered but not connected.)		
55	UART2_RTS	Output	UART2 Request to Send (CLI port)		
56	ADC1/GPIO2	Input/Output	Auxiliary Analog to Dig- ital Converter Input/Pro- grammable GPIO		
57	GND	Supply	Negative supply voltage		
58	STATUS	Output	Module Status		
59	ADC0/GPIO1	Input/Output	Auxiliary Analog to Digi- tal Converter Input /Pro- grammable GPIO		
60	UART1_TX	Output	UART1 Transmit Data (Mo- dem Log port)		
61	UART1_RTS	Output	UART1 Request to Send (Modem Log port)		
62	RESERVED	_	Reserved		
63	UART1_RX	Input	UART1 Receive Data (Mo- dem Log port)		
64	RESERVED	_	Reserved (Shall be sol- dered but not connected.)		
65	UART1_CTS	Input	UART1 Clear to Send (Mo- dem Log port)		
66	RESERVED	_	Reserved (Shall be sol- dered but not connected.)		
67	RESERVED	_	Reserved (Shall be sol- dered but not connected.)		
68	RESERVED	_	Reserved (Shall be sol- dered but not connected.)		
69	RESERVED	_	Reserved (Shall be sol- dered but not connected.)		
70	RESERVED	_	Reserved (Shall be sol- dered but not connected.)		
71	RESERVED	_	Reserved (Shall be sol- dered but not connected.)		
72	VSIM	Output	SIM Output voltage		
73	RESERVED	_	Reserved (Shall be sol- dered but not connected.)		

Table 18: Pinout2



Pin Number	Designation	I/O	Description	
74	SPIM1_MISO/GPIO39	Input/Output	MCU_SPIM1_MISO/ Programmable GPIO	
75	SIMCLK	Output	SIM Clock	
76	SPIM1_CLK/GPIO41	Input/Output	MCU_SPIM1_CLK/ Programmable GPIO	
77	SIMRST	Output	SIM Reset	
78	RESERVED	-	Reserved (Shall be sol- dered but not connected.)	
79	SIMIO	Input/Output	SIM Data	
80	VCAP	Input/Output	Connecting external ca- pacitor as backup for VDD	
81	SPIM1_EN/GPIO40	Input/Output	MCU SPI Enable/ Programmable GPIO	
82	DEBUG_RST	Input/Output	Reset pin for the JTAG probe	
83	SPIM1_MOSI/GPIO38	Input/Output	MCU_SPIM1_MOSI/ Programmable GPIO	
84	DEBUG_SEL	Input	Reset pin for the JTAG probe	
85	VBACKUP	Input	Input from backup battery	
86	GND	Supply	Negative supply voltage	
87	VDDIO	Output	Output Voltage (it will turn off at DH0 and DH1 sleep mode)	
88	GND	Supply	Negative supply voltage	
89	RESERVED	-	Reserved (Shall be sol- dered but not connected.)	
90	GND	Supply	Negative supply voltage	
91	RESERVED	_	Reserved(Shall be sol- dered but not connected.)	
92	GND	Supply	Negative supply voltage	
93	GND	Supply	Negative supply voltage	
94	GND	Supply	Negative supply voltage	
95	GND	Supply	Negative supply voltage	
96	GND	D Supply Negative supply voltage		
97 GND		Supply	Negative supply voltage	

Table 19: Pinout3



Pin Number	Designation	I/O	Description	
98	GND	Supply	Negative supply voltage	
99	GND	Supply	Negative supply voltage	
100	GND	Supply	Negative supply voltage	
101	GND	Supply	Negative supply voltage	
102	GND	Supply	Negative supply voltage	
103	GND	Supply	Negative supply voltage	
104	GND	Supply	Negative supply voltage	

Table 20: Pinout4

3.1 Module Power Up

An automatic power up sequence occurs when connecting the device to the power supply (VDD). The automatic power up sequence consists of the following phases:

- Phase 0: RET LDO to ramp up for supplying 1.0V retention core domain.
- Phase 1: IO LDO to ramp up for supplying 1.8 V IO domain.
- Phase 2: RF LDO to ramp up for supplying 1.9V RF domain.
- Phase 3: DCDC to ramp up for supplying 1.3V of Digital LDO and RF.
- Phase 4: DIG LDO to ramp up for supplying 1.0V of digital core domain.
- Phase 5: FLASH LDO to ramp up for supplying 1.8 V of Flash Domain.

Regulators will start ramping only with 1us delay from power good indication of previous phase. The automatic power up sequencing is shown below:

Parameter	Description	Min.	Max.	Unit
t1	When VDD crosses the 0.8V threshold-VRTC should follow the VDD unless it has some capacitance on it.	0	5	μs
t2	Digital retention power up, the VDD slew rate has impact on this timing.	70	100	μs
t3	IO LDO power up.	10	60	μs
t4	RF LDO power up.	10	60	μs
t5	DCDC boot time.	100	200	μs
t6	Core LDO power-up.	10	60	μs
t7	FLASH LDO power-up.	10	60	μs





Figure 8: Adrastea-I Power up Sequence

3.2 Module Power Down

Power down sequence of the regulators will occur in following conditions:

- Turn off VDD.
- Shutdown is requested by /RESET pin pulled to low.

3.3 Module Reset

Module reset will occur in following conditions:

- Perform power cycle Turn off/on VDD and power up the device from reset state.
- Using /RESET pin user can initiate power cycle that resets the device.



3.4 WAKEUP pin

This pin can be used to immediately wake up the module when being in low power state. This pin allows the module to get out of sleep mode when pulled HIGH.

The host connected to this pin should always keep the state of this pin (HIGH/LOW) at a known state (not floating) according to the required functionality.

- Pulled HIGH: Wake up internal MCU of module from sleep mode.
- Pulled LOW: Allowing internal MCU of module to go into sleep mode.

3.5 AT_IN and AT_OUT pins

User can connect the AT_OUT pin to the AT_IN pin in order to protect a device or module from tampering. The device will generate a software indication if the AT_OUT and AT_IN pins are disconnected.

The anti-tampering mechanism works in all active modes and all DHx power saving modes. If the anti-tampering is not in use, the AT_IN should be shorted to GND.

3.6 /RESET pin

This pin has the highest priority compared to other chip functionalities, therefore asserting it will always force a hard reset. This pin is with internal PU resistor to 1.8V.

- Pulled HIGH: Turn on module regulators and power up the module.
- Pulled LOW: Turn off module regulators and shutdown the module.
- LOW to HIGH: Reset module (keep holding for at least 100ms on LOW level before changing to HIGH).



3.7 EXT_ALARM pin

The EXT_ALARM pin can be used as an alarm indicator to an external host as per the Adrastea-I power mode. The behavior is as below:

Module State	Test Condition	EXT_ALARM Pin Expected behavior	
DH0 MCU Shutdown, AT+CFUN=0		High Impedance	
DH1	MCU Shutdown, AT+CFUN=0	High Impedance	
DH2	MCU Shutdown, AT+CFUN=0	LOW signal	
Active	MCU RUN	HIGH signal	

Table 22: EXT_ALARM Pin

3.8 RF_LTE pin

This is the LTE antenna pin. The impedance should be close to 50 Ω , VSWR (Voltage Standing Wave Ratio) < 1.5.

Connect 50 Ω transmission lines from this pin to the 50 Ω Primary Antenna/Antenna-connector. Please refer to our hardware layout recommendations (chapter 7).

3.9 RF_GNSS pin

This is the GNSS antenna pin. The impedance should be close to 50 Ω , VSWR (Voltage S-tanding Wave Ratio) < 1.5.

Connect 50 Ω transmission lines from this pin to the 50 Ω Primary Antenna/Antenna-connector. Please refer to our hardware layout recommendations (chapter 7).

3.10 VBACKUP and VCAP pins

Adrastea-I supports a battery backup mechanism which allows seamless replacement of a weak battery. The battery should be replaced after the device is placed in DH0 state, and only when the RTC circuitry is operational, and is applied by VRTC.

The VBACKUP pin (battery) or the VCAP (capacitor) can be used as a backup during replacement. The VCAP pin should be left floating if a battery backup is used, while the VBACKUP pin should be left floating if a capacitor backup is used. If the application does not require a battery then both the VBACKUP and the VCAP pins should be left floating.



3.10.1 VCAP pin

The capacitor value should be large enough to keep the VCAP supply voltage above 1.8 V for as long as it takes for the battery to be replaced. Equation 1 should be used for calculating the capacitor value (C_{CAP}).

Equation1: $C_{CAP} = (I_{CAP} \times T)/(V_{to} - V_{MIN})$

The following parameters should be taken into account when making these calculations:

- The maximum current drawn from VCAP ($I_{CAP} = 10uA$).
- The maximum period of time (T) it should take for battery replacement.
- The voltage that the capacitor was charged to (V_{to}).
- The minimum voltage that the capacitor can discharge while still providing sufficient operational voltage for the RTC (V_{MIN} = 1.8 V).

Example:

If the capacitor is charged to 3.3 V, and battery replacement requires 30 seconds, then the capacitor should be at least 200 μ F (see equation below). $C_{CAP} = (10uA \times 30s)/(3.3 V - 1.8 V) = 200uF$

3.10.2 VBACKUP pin

There is an option to include an external battery that can maintain the system's supply for a very short time while the main supply (VDD) is absent. The intention is to use a coin battery which is non-rechargeable. VDD thresholds at which the capacitor will start to provide VRTC:

- Similar to VCAP thresholds (see in the above section 3.10.1).
- Pull Low: Turn off module regulators and shutdown the module.
- In case a battery is not used, this pin should be left open (not connected).

3.10.3 VDDIO

1.8 V power to the retention's IO.



VDDIO is turned off in DH0 and DH1 state. Therefore it is not allowed to provide external voltage to IOs.



3.11 E-JTAG Debug port

The Adrastea-I supports an E-JTAG interface for MCU debugging.

	Pin Number	Designation	Description	
10 EJ_TCK JTAG Test Clock		JTAG Test Clock		
	12	EJ_TDO	JTAG Test Data Output	
14 EJ_TDI JTAG Test Data Input 16 EJ_TMS JTAG Test Mode Select 18 EJ_TRST JTAG Test Reset (Required external Pull down		JTAG Test Data Input		
		JTAG Test Mode Select		
		JTAG Test Reset (Required external Pull down)		
	84	DEBUG_SEL	HW Pin for EJTAG chain selection	

The E-JTAG interface includes the following pins:

Table 23: E-JTAG Debug port

These pins are not multiplexed with other interfaces in order to save them for debug purposes. The debug port can be directed in direct line to the modem debug chain or MCU. The default direction is set according to the external pin state (DEBUG_SEL). The DEBUG_SEL has an internal Pull Down by default.



Adrastea-I has an internal PD for EJ_TRST, as it is a very sensitive line (in case it will toggle high the processor will enter debug mode), we suggest not keeping it unconnected but to connect it to an external 10K Ω PD. Other E-JTAG pins can be kept NC.



3.12 GPIO Pin Information

Pin Number	Designation	Description
56	ADC1/GPIO2	Auxiliary Analog to Digital Converter Input /Programmable GPIO
59	ADC0/GPIO1	Auxiliary Analog to Digital Converter Input /Programmable GPIO
74	SPIM1_MISO/GPIO39	MCU_SPIM1_MISO/Programmable GPIO
76	SPIM1_CLK/GPIO41	MCU_SPIM1_CLK/Programmable GPIO
81	SPIM1_EN/GPIO40	MCU SPI Enable/Programmable GPIO
83	SPIM1_MOSI/GPIO38	MCU_SPIM1_MOSI/Programmable GPIO

Table 24: GPIO Pin Information

3.13 Digital IO Pins Specifications

These characteristics are applicable for VDDIO in the 1.7V - 1.9V range.

Parameter	Min.	Max.	Unit
Input LOW Level, input and I/O pins	GND	0.3 x VDDIO	V
Input HIGH Level, input and I/O pins	0.7 x VDDIO	VDDIO	V
Output LOW Level		0.2 x VDDIO	V
Output HIGH Level	0.8 x VDDIO		V
Input pull-up resistor resistance	13	45	KΩ
Input pull-up resistor current	11	44	μA
Input pull-down resistor resistance	13.6	45	KΩ
Input pull-down resistor current	11	43	μA

Table 25: Digital IO Pins Specifications



The total current from all IOs combined, and supplied by VDDIO, should not exceed 50mA.
User manual Adrastea-I

4 Module Interfaces

Adrastea-I interfaces and specific pin connections for different interfaces are described in this chapter.

4.1 UART Interface

Adrastea-I supports 3 UART interfaces.

UART Number	Description
UART0	MCU UART, this interface is used for AT Commands.
UART1	This interface is used to capture modem logs.
UART2	This interface is used for MCU and Modem Firmware upgrade

Table 26: UART Interfaces

4.1.1 UART Default Configuration

UART	Function	Baud rate	Data	Parity	Stop	Flow Control
UART0	MCU UART	115200	8bit	None	1bit	Hardware RTS/CTS (default None)
UART1	Modem Log Port	921600	8bit	None	1bit	Hardware RTS/CTS (default None)
UART2	Firmware upgrade (CLI Port)	115200	8bit	None	1bit	Hardware RTS/CTS (default None)

Table 27: UART Default Configuration



UART1: Is used to capture the modem logs. UART2: Is used for local firmware upgrade.



Flow control is needed for firmware upgrade.





UART communication is not possible when Adrastea-I is in deep hibernate mode (DH0, DH1 and DH2)

4.1.2 UART0 Pin Interface

Pin Number	Designation	I/O	Description	Electrical Characteristic
19	UART0_RTS	Output	MCU UART0 Request to Send	1.8 V
20	UART0_CTS	Input	MCU UART0 Clear to Send	1.8 V
21	UART0_TX	Output	MCU UART0 Transmit Data	1.8 V
22	UART0_RX	Input	MCU UART0 Receive Data	1.8 V

	Table	28:	UART0	Pin	Interface
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Electrical characteristics (operation voltage) of UART0 pins are 1.8 V.

4.1.3 UART1 Pin Interface

Pin Number	Designation	I/O	Description	Electrical Characteristic
61	UART1_RTS	Output UART1 Request to Send (Modem Log port)		1.8 V
65	UART1_CTS	Input	UART1 Clear to Send (Modem Log port)	1.8 V
60	UART1_TX	Output	UART1 Transmit Data (Modem Log port)	1.8 V
63	UART1_RX	Input	UART1 Receive Data (Modem Log port)	1.8 V

Table 29: UART1 Pin Interface



Electrical characteristics (operation voltage) of UART1 pins are 1.8 V.



4.1.4 UART2 Pin Interface

Pin Number	Designation	I/O	Description	Electrical Characteristic
55	UART2_RTS	Output	UART2 Request to Send (CLI port)	1.8 V
53	UART2_CTS	Input	UART2 Clear to Send (CLI port)	1.8 V
48	UART2_TX	Output	UART2 Transmit Data (CLI port)	1.8 V
50	UART2_RX	Input	UART2 Receive Data (CLI port)	1.8 V

Table 30: UART2 Pin Interface



Electrical characteristics (operation voltage) of UART2 pins are 1.8 V.

4.1.5 UART0 Host Connection

Connection to host is possible through UART0. This section describes the external host interface which is used to control the modem.



Electrical characteristics (operation voltage) of UART0 pins are 1.8 V.

Below figure shows TX/RX/CTS and RTS connections based on 1.8 V I/O level of external host.





Figure 9: UART0 Host Interface



4.2 SPI Interface



The SPI interface is available when using a customized firmware. It is not implemented within the Adrastea-I default MCU firmware.

4.2.1 SPIM Pin Interface



Electrical characteristics (operation voltage) of SPIM pins are 1.8 V.

Pin Number	Designation	Description	Тур.	Unit
83	SPIM_MOSI	SPIM_MOSI connect to SPI Slave SDI	1.8	V
74	SPIM_MISO	SPIM_MISO connect to SPI Slave SDO	1.8	V
76	SPIM_CLK	SPIM_CLK connect to SPI Slave CLK	1.8	V
81	SPIM_EN	SPIM_EN connect to SPI Slave CS	1.8	V

Table 31: SPIM Pin Interface

4.2.2 SPIM Connection



Electrical characteristics (operation voltage) of SPIM pins are 1.8 V.

User manual Adrastea-I





Figure 10: SPIM Connection



4.3 I²C Interface

Adrastea-I provides an I^2C interface with clock rate up to 400 kbps. Its operation voltage is 1.8 V.



This interface is enabled but connecting to the external device is subjected to a customized firmware and not supported by the default firmware.

4.3.1 I²C Pin Interface



Electrical characteristics (operation voltage) of I²C pins are 1.8 V.

Pin Number	Designation	Description	Тур.	Unit
15	I2C_SCL	I ² C SCL connect to external device SCL	1.8	V
17	I2C_SDA	I ² C SDA connect to external device SDA	1.8	V

Table 32: I²C Pin Interface

4.3.2 I²C Connection



Electrical characteristics (operation voltage) of I²C pins are 1.8 V.

WIRELESS CONNECTIVITY & SENSORS







Figure 11: I²C Connection

User manual Adrastea-I

4.4 ADC Interface

Adrastea-I includes two auxiliary A/D converters to sense external analog inputs.



Electrical characteristics (operation voltage) of ADC pins are 1.8 V.

ADC Interface	Description	Min	Max.	Unit
ADC0	Auxiliary Analog to digital converter channel 0	0	1.8	V
ADC1	Auxiliary Analog to digital converter channel 1	0	1.8	V

Table 33: ADC Interfaces

4.4.1 ADC Functional Specifications

Symbol	Parameter	Min	Тур.	Max	Unit
N	Resolution	6		12	Bits
F _{CLK}	Clock rate	4	40	52	MHz
F _S	Conversion rate per channel (Note1)		F _c /(N+3)		MSPS
V _{IN}	Input voltage range		1.8		V
INL	Integral Nonlinearity		±1	± 2	LSB
DNL	Differential Nonlinearity	-0.9		0.9	LSB
R _{IN}	Input resistance (Note3)			1.42	MΩ
C _{IN}	Input capacitance during sampling	2.6			pF

Table 34: ADC Functional Specifications

Note1: The general formula for this conversion rate is: $F_S = F_{CLK} / (N+3) / N$ umber of sources. Note2: Conversion rate at 3.46 MSPS and 12bit resolution.

Note3: Measured Input resistance and current on ADC0 with different voltage labels are as below:



Input Voltage (V)	Input Resistance (M Ω)	Measured Current (µA)
1.0	0.98	1.02
1.5	1.42	1.07
1.7	1.38	1.23

Table 35: Measured Input Resistance

4.4.2 ADC Pin Interface

Pin Number	Designation	Description
56	ADC1/GPIO2	Auxiliary Analog to Digital Converter Input /Programmable GPIO
59	ADC0/GPIO1	Auxiliary Analog to Digital Converter Input /Programmable GPIO

Table 36: ADC Pin Interface

4.5 SIM Interface

Adrastea-I supports 1.8 V SIM Cards.

4.5.1 SIM Pin Interface



Electrical characteristics (operation voltage) of SIM pins are 1.8 V.

Pin Number	Designation	Description
72	VSIM	SIM Output voltage
75	SIMCLK	SIM Clock
77	SIMRST	SIM Reset
79	SIMIO	SIM Data

Table 37: SIM Pin Interface



4.6 RF interfaces

Pin Number	Designation	Description
39	RF_LTE	RF Signal LTE (The impedance (S11) should be close to 50 Ω , VSWR < 1.5 Please refer to our hardware layout recommendations (chapter 7).
43	RF_GNSS	RF Signal GNSS (The impedance (S11) should be close to 50 Ω , VSWR < 1.5 Please refer to our hardware layout recommendations (chapter 7).

Table 38: RF Pin Interface

4.7 E-JTAG Debug port

The Adrastea-I supports an E-JTAG interface for MCU debugging.

The E-JTAG Interface includes the following pins	The E	E-JTAG	interface	includes	the	following	pins:
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Pin Number	Designation	Description
10	EJ_TCK	JTAG Test Clock
12	EJ_TDO	JTAG Test Data Output
14	EJ_TDI	JTAG Test Data Input
16	EJ_TMS	JTAG Test Mode Select
18	EJ_TRST	JTAG Test Reset (Required external Pull down)
84	DEBUG_SEL	HW Pin for EJTAG chain selection

Table 39: E-JTAG Debug port

These pins are not multiplexed with other interfaces in order to save them for debug purposes. The debug port can be directed in direct line to the modem debug chain or MCU. The default direction is set according to the external pin state (DEBUG_SEL). The DEBUG_SEL has an internal Pull Down by default.



Adrastea-I has an internal PD for EJ_TRST, as it is a very sensitive line (in case it will toggle high the processor will enter debug mode), we suggest not keeping it unconnected but to connect it to an external 10K ohm PD. Other E-JTAG pins can be kept NC.



4.8 GPIO Pin Information

Pin Number	Designation	Description
56	ADC1/GPIO2	Auxiliary Analog to Digital Converter Input /Programmable GPIO
59	ADC0/GPIO1	Auxiliary Analog to Digital Converter Input /Programmable GPIO
74	SPIM1_MISO/GPIO39	MCU_SPIM1_MISO/Programmable GPIO
76	SPIM1_CLK/GPIO41	MCU_SPIM1_CLK/Programmable GPIO
81	SPIM1_EN/GPIO40	MCU SPI Enable/Programmable GPIO
83	SPIM1_MOSI/GPIO38	MCU_SPIM1_MOSI/Programmable GPIO

Table 40: GPIO Pin Information



5 Functional description

The Adrastea-I LTE-M/NB-IoT module is intended to be used as a radio sub-system in order to provide LTE-M/NB-IoT communication capabilities to the system.

The Adrastea-I modem firmware is 3GPP Release 13 compliant, which is upgradable to Release-14.

The UART-0 acts as the primary interface between the module and a host micro-controller. The module can be controlled and operated using a set of AT-commands over UART-0.

Adrastea-I is a high-performance, multi-band dual mode LTE-M/NB-IoT module with ultra-low power consumption.

Embedded GNSS allows location applications to track positioning.

An integrated application MCU is available for customer applications.

5.1 Adrastea-I State Transition



Figure 12: Adrastea-I State Transition



5.2 Adrastea-I Power Saving Modes

This section summarizes the various low power operating modes of the Adrastea-I module.



The Adrastea-I selects the described power modes according to the the maximum allowed chip power mode configuration. The currently configured power mode can be checked with AT command: at%getacfg="pm.conf.max_allowed_pm_mode"

5.2.1 DH0 Mode

DH0 mode provides long entry and recovery times and is mainly used for very long inactivity intervals like power saving mode. In this mode all digital logic is powered down, memories are not retained, IO are not stored.

This is the lowest power mode of the system.

One of the following dedicated actions is used to wake up from this mode:

- WAKEUP (Wakeup active high).
- Module reset (/RESET Reset active low).
- Module power down.



In this mode VDDIO is turned off, therefore it is not allowed to provide external voltage to IOs that are not defined as a wake up source in the list above

5.2.2 DH1 Mode

All digital logic is powered down, a configurable amount of retention memory is retained (64KB granularity), IOs are not stored.

One of the following dedicated actions is used to wake up from this mode:

- WAKEUP (Wakeup active high).
- Module reset (/RESET Reset active low).
- Module power down.

A Wakeup event initiates a boot flow. This mode is similar to DH2; however, lower power consumption due to IO logic unretained.





In this mode VDDIO is turned off, therefore it is not allowed to provide external voltage to IOs that are not defined as a wake up source in the list above

5.2.3 DH2 Mode

Achieve the lowest power consumption while retaining the content of SRAM and registers. All digital logic is powered down.

One of the following dedicated pins is used to wake up from this mode:

- WAKEUP (Wakeup active high).
- Module reset (/RESET Reset active low).
- Module power down.

Wakeup event initiates a boot flow. This mode is similar to DH1; however, it also enables output IOs to latch and wakeup from digital inputs.



Adrastea-I is set by default in DH2 state.

5.3 GNSS Receiver

Adrastea-I supports GPS and GLONASS satellite systems using dedicated hardware accelerators in a power and cost efficient manner. The GNSS receiver shares certain hardware resources with the modem. This enables GNSS measurement slots to be efficiently scheduled based on the modem link state. The device key target is to allow GNSS positioning for asset management applications where infrequent position updates are required. External LTE and GNSS antennas are required.

5.3.1 Supported GNSS constellations

Adrastea-I supports the following constellation combinations:

- GPS
- GLONASS

5.3.2 GNSS Co-existence with LTE Modem

The Adrastea-I GNSS shares the RF Rx path with the LTE modem and, therefore, cannot operate in parallel with LTE data transfer. Hence this GNSS is not suitable for products that inherently require this co-existence, LTE connection and GNSS tracking.



GNSS cannot co-exist with LTE data transfer. LTE communication has higher priority over GNSS and, therefore, GNSS is automatically shut down once LTE is active (if it was active). While LTE is active, GNSS cannot be activated and all GNSS AT commands are responded with error.

5.4 Application MCU

This section provides information on the User MCU subsystem. This MCU is exclusively for customer applications.

- ARM Cortex-M4 MCU
- Flash size: 1 MB
- RAM Size: 256 KB

5.4.1 Application MCU Software Development Kit

The MCU SDK allows software developers to write their own applications directly onto the ALT1250 internal application MCU with no need to write code into the ALT1250 Modem Application Processor (MAP).



MCU has default PowerManager firmware. PowerManager example demonstrates how MCU sleep (power save) works.



The "map" command is required before sending AT commands to modem.

The SDK can be downloaded from *https://developer.sony.com/*. To get access to the portal, Follow below procedure:

• Fill the Sony MCU access request form: https://bit.ly/44lqgKD



Important to fill in Module vendor "Wurth Elektronik" at 6 in a link above.

• Sony receives and process the request , Sony will provide 7 digit registration number to email id provided in above form.

WIRELESS CONNECTIVITY & SENSORS





Please note completion time for this request is 3-5 working days.

• With 7 digit registration number, access below link and getting right into the Sony MCU portal.

https://developer.sony.com/develop/cellular-iot/register.

Email	
Password	
Retype password	
First name	
Last name	
Company name	
Enter the registration number:	
I have read and agree to the Terms of Use and Privacy Policy of Sony's Dev	veloper World
I have read and agree to the Terms of Use of Sony Semiconductor Israel	
Register	

Figure 13: Adrastea-I: Sony MCU portal registration



Some information provided in this document can change. Please refer to the link for latest information *https://developer.sony.com/develop/cellular-iot/how-to-register*



- Login into sony portal *https://developer.sony.com/* using credentials created in above steps.
- Click on "Develope->IoT->Altair development portal".



Figure 14: Adrastea-I: Sony MCU portal Access



Adrastea-I MCU is verified with Sony MCU SDK version 2.1. Refer documentation for MCU SDK version 2.1

 To access documentation of SDK version 2.1 click below link (Note: Login into portal is required to access below link). https://bit.ly/3Id8kse



6 Quick start guide

It is recommended to use the Adrastea-I evaluation kit and Adrastea Commander tool for putting the LTE-M/NB-IoT module into operation. The evaluation kit has external GNSS and LTE antennas. Please refer to the [2] for detailed information.

6.1 Minimal pin connections

The following image shows the steps to be performed to integrate the Adrastea-I into a custom end device.



Figure 15: Minimal pin connections

1. Supply voltage and ground Connect the *VDD*, *VDD_FEM* and *GND* pins to supply the radio module with power.



Please note the minimum voltage acceptance difference between *VDD* and *VDD_FEM*.

- MCU UART0 serial interface to the host Connect the UART pins UART0_RX and UART0_TX to the host to control the module via host controller.
- 3. Reset

Connect the /RESET pin to the host to allow a hard reset of the module.



- 4. Wakeup Connect the *WAKEUP* pin to the host to allow the waking-up function of the module.
- 5. Antenna connection connect the *RF_LTE* pin to an external LTE antenna. Connect the *RF_LTE* pin to an external GNSS antenna.
- 6. SIM card connection connect the followings pins to a proper SIM card holder to allow network connection: *VSIM*, *SIMCLK*, *SIMIO* and *SIMRST*.
- 7. (Optional) MCU UART1 serial interface for modem logs Connect the UART pins *UART1_RX* and *UART1_TX* to obtain modem logs.
- (Optional) MCU UART2 serial interface for firmware update Connect the UART pins UART2_RX, UART2_TX, UART2_CTS and UART2_RTS to execute firmware updates.
- 9. (Optional) Status indication Connect the *STATUS* pin to the host controller to allow easy indication of the status.



The logic level of the module is based on 1.8 V. A 3.3 V logic level shall not be connected directly to the digital interfaces of the module

If the module has to be connected to a PC, a converter (TTL to RS-232 or TTL to USB) has to be used. See chapter Pinout for details on all pins. Please refer to the Adrastea-I evaluation board schemes for a Reference design.

6.2 Prerequisites

- 1. Adrastea-I Evaluation Kit.
- 2. Computer with a serial terminal emulator. The use of Würth Elektronik eiSos's Adrastea Commander is recommended ([1]).
- 3. Install on your PC the corresponding FTDI driver package. Click on link 1 (FTDI drivers) in the "Adrastea Commander" tool or download direct from *https://www.ftdichip.com/Drivers/VCP.htm*.
- 4. A valid NB-IoT and LTE-M enabled nano SIM card. To order IoT SIM cards click on link 2 (Get your SIM card) in the "Adrastea Commander" tool or order directly from *https://iotcreators.com/wuerth/*.





Figure 16: Adrastea Commander

Me Adrastea Commander			- 🗆 X
Application GNSS Data usage estimat Module Status Serial No.: Sim card: NotInserted Network: Not Available C. Get vour SIM card, Run sequence G	ion Support COM settings COM settings COM settings Connect ETDL drivers AT+CGMI Wurth Elektronik eiSos OK AT+CGMM WIRL-CLTI-ADRASTEA-I OK Attick selection [Not set] [Controls Clear Copy Save Send [Not set]	Command groups New Collaps Expand
	[Not set] [Not set]	[Not set]	





6.3 Taking into operation

- 1. Insert a valid NB-IoT and LTE-M enabled nano SIM card.
- 2. Connect LTE and GNSS external antennas provided with the Evaluation Kit.
- 3. Connect the power jack or external power supply to the EV board and verify that the VDD is stable and able to reliably supply the module's static and peak current consumption, as specified in the data sheet and user manual.
- 4. Connect the evaluation board to the PC using a USB-cable. Four COM ports should be detected and installed on your PC. Check the device manager to acquire the COM port names of the EV board. A typical name is "COMxy" in Windows systems or /dev/ttyUSB0 in Linux systems.

!	Note that usually the four COM ports are assigned in ascendir shown in figure 18	ng orde	r, e	35
Marastea Commander		_		\times

Application GNSS Support					
Module Status Serial No.: Sim card: NotInserted Network: Not Available Get your SIM card.	Console COM settings Port: COM57 COM57 COM58 COM59 COM50	Baud rate: 115200 V ect and access COM ports.	Connect Controls Clear Copy	Run sequence Save	Commands Command groups New Collaps Expand
	Quick selection				
	AT%MEAS="4"	AT%MEAS="8"	AT+CPIN?	AT+CFUN=0	
	AT%TSTRF=1	AT%MEAS="96"	AT%PINGCMD=0,"8.8.8.8",	at%cmatt=1	

Figure 18: COM ports detected - Adrastea commander



To interact with the module, it is advised to use the Adrastea Commander tool. Otherwise, a terminal program (like "PuTTY" or "Tera Term" for Windows) has to be run and the corresponding COM port has to be opened using the default settings of the mounted Adrastea-I module.

- 5. Press the reset button on the Evaluation board to ensure a clean start-up of the module. See figure 19.
- 6. Type and enter the "map" command, this command is required before sending AT commands to modem.



Ve Adrastea Commander	- 🗆 X
Application GNSS Data usage estimation Support	
Application GNSS Data usage estimation Support Module Status Serial No: [132000082] Sin card: Ready Network: Not Available Get our SIM card. Run sequence Net Get our SIM card. Run sequence ProverManager Compiled on Jun 4 2021 at 03:45:58 MCU D2_01_00_00_5LO RD6005@041505 ProverManager Compiled on Jun 4 2021 at 03:45:58 MCU menu - PowerManager ProverManager Compiled on Jun 4 2021 at 03:45:58 MCU menu - PowerManager ProverManager Compiled on Jun 4 2021 at 03:45:58 MCU menu - PowerManager ProverManager Compiled on Jun 4 2021 at 03:45:58 MCU menu - PowerManager ProverManager Compiled on Jun 4 2021 at 03:45:58 MCU menu - PowerManager ProverManager Compiled on Jun 4 2021 at 03:45:58 MCU menu - PowerManager ProverManager Compiled on Jun 4 2021 at 03:45:58 MCU menu - PowerManager ProverManager Compiled on Jun 4 2021 at 03:45:58 MCU menu - PowerManager ProverManager Compiled on Jun 4 2021 at 03:45:58 MCU menu - PowerManager ProverManager Compiled on Jun 4 2021 at 03:45:58 MCU menu - PowerManager ProverManager Compiled on Jun 4 2021 at 03:45:58 MCU menu - PowerManager ProverManager Compiled on Jun 4 2021 at 03:45:58 MCU menu - PowerManager ProverManager Compiled on Jun 4 2021 at 03:45:58 MCU menu - PowerManager ProverManager Compiled on Jun 4 2021 at 03:45:58 MCU menu - PowerManager ProverManager Compiled on Jun 4 2021 at 03:45:58 MCU menu - PowerManager ProverManager Compiled on Jun 4 2021 at 03:45:58 MCU menu - PowerManager ProverManager Compiled on Jun 4 2021 at 03:45:58 MCU menu - PowerManager ProverManager Compiled on Jun 4 2021 at 03:45:58 MCU menu - PowerManager ProverManager Compiled on Jun 4 2021 at 03:45:58 MCU menu - PowerManager ProverManager Compiled Diverment ProverManager Compiled Diverment ProverManager Compiled Diverment ProverManager Compiled Diverment ProverManager Compiled ProverManager ProverManager Compiled Diverment ProverManager Compiled ProverManager ProverManager Compiled ProverManager ProverManager Compiled ProverManager ProverManager Compiled ProverManager ProverManager Compiled ProverMana	Commands Command groups New Collaps Expand General B-GNSS
Send	
Quick selection	
[Not set] [Not set] [Not set]	
[Not set] [Not set] [Not set]	

Figure 19: MiniConsole start view - Adrastea Commander



The "map" command is required before sending AT commands to modem.



When the AT Command UART port is opened, the Adrastea-I output console displays: %SCMNOTIFYEV:"ADRASTEA-IReady".

7. Check if the SIM card is detected. Send command MAP follow by the command AT+CPIN?. See figure 20.

WIRELESS CONNECTIVITY & SENSORS User manual Adrastea-I



🚾 Adrastea Commander	-
Application GNSS Support	
Module Status Console Serial No.: Unknown Image: Common commo	Controls Cear Copy Save Cear Copy Save Centrol Cear Copy Save Collaps Expand Expend Expen

Figure 20: SIM card detected - Adrastea Commander

User manual Adrastea-I

6.4 Select LTE-M or NB-IoT Mode

Adrastea-I supports AT Commands for LTE-M and NB-IoT selection. AT Command AT%RATACT is used to Switch/Select the LTE-M or NB-IoT.



Note: The default mode for the Adrastea-I module is LTE-M single mode



Any attempt to switch to the mode already in use will be ignored and OK will be returned.

1. Select Relevant RAT:

The following AT command will change the module mode to NB-IoT.

AT%RATACT="NBIOT",1 OK

The following AT Command can be used to verify that NB-IoT has been selected.

```
AT%RATACT?
%RATACT: "NBIOT",1,0
OK
```

The following AT command will change the module mode to LTE-M.

AT%RATACT="CATM",1 OK

The following AT Command can be used to verify that LTE-M. has been selected.

AT%RATACT? %RATACT: "CATM",1,0 OK

2. Reset the device:

The following AT Command is used to reset the device.

ATZ			
OK			



6.5 Register to Network



The configurations "Select LTE-M or NB-IoT Mode" (see Chapter 6.4) should be done before registering to the LTE network.



A valid LTE-M/NB-IoT SIM card should be inserted, check SIM status with AT+CPIN? AT Command.

The registration process in LTE-M and NB-IoT technologies could take some minutes to complete. This happens especially in case of the very first registration: new SIM, new location, new module. This is because of scanning of available frequencies and selection of a suitable frequency.

1. Check SIM status:

The following command is used to read the SIM status.



2. To start the registration procedure:

The following command will trigger the registration procedure with the network.



 Enable network registration unsolicited result code: The following command will enable network registration and location information unsolicited result code.



4. Read the network registration status:

The following command will read the network registration status.





The following command will trigger the de-registration procedure with the network.



6.6 Activate GNSS

This section shows how to enable the GNSS feature of the Adrastea-I module.



GNSS cannot co-exist with LTE data transfer. LTE communication has higher priority over GNSS and, therefore, GNSS is automatically shut down once LTE is active (if it was active). While LTE is active, GNSS cannot be activated and all GNSS AT commands are responded with error.

1. Disable LTE prior to activating GNSS:

The following command will disable LTE radio.



2. Allow unsolicited notifications:



3. Get available satellites:



It is necessary to check that there are at least 4 satellites available with an SNR>25.



AT%IGNSSINFO="SAT"	
%IGNSSINFO: 11	
%IGNSSINFO:03,36,294,49	
%IGNSSINFO:06,53,263,50	
%IGNSSINFO:14,42,180,50	
%IGNSSINFO:15,13,042,50	
%IGNSSINFO:16,08,251,50	
%IGNSSINFO:18,56,044,50	
%IGNSSINFO:19,25,314,50	
%IGNSSINFO:21,46,104,51	
%IGNSSINFO:22,71,306,49	
%IGNSSINFO:24,14,080,49	
%IGNSSINFO:27,51,282,50	

4. Enable NMEA sentences (This command is required only when messages are required in GNSS tab of Adrastea Commander tool):

AT%IGNSSCFG="SET","NMEA","GGA","GSA","GSV","GNS","RMC" OK

5. Start GNSS:



For first time GNSS fix, cold start should be triggered to start GNSS

The following command is used for cold GNSS start.

AT%IGNSSACT=1,1

OK

The following command is used for hot GNSS Start.

AT%IGNSSACT=1,2

OK

6. Get fix:

AT%IGNSSINFO="FIX"

%IGNSSINFO: 2,"11:17:02","04/05/2020","32.195970","34.892572"," -10.500000",1588580222000,1,"0.000000","B"



The following AT command is used to stop GNSS functionality:

AT%IGNSSACT=0

OK



7 Design in guide

7.1 Advice for schematic and layout

For users with less RF experience it is advisable to closely copy the relating evaluation board with respect to schematic and layout, as it is a proven design. The layout should be conducted with particular care, because even small deficiencies could affect the radio performance and its range or even the conformity.

The following general advice should be taken into consideration:

- A clean, stable power supply is strongly recommended. Interference, especially oscillation can severely restrain range and conformity.
- Variations in voltage level should be avoided.
- LDOs, properly designed in, usually deliver a proper regulated voltage.
- Blocking capacitors and a ferrite bead in the power supply line can be included to filter and smoothen the supply voltage when necessary.



No fixed values can be recommended, as these depend on the circumstances of the application (main power source, interferences etc.).



The use of an external reset IC should be considered if one of the following points is relevant:

- The slew rate of the power supply exceeds the electrical specifications.
- The effect of different current consumptions on the voltage level of batteries or voltage regulators should be considered. The module draws higher currents in certain scenarios like start-up or radio transmit which may lead to a voltage drop on the supply. A restart under such circumstances should be prevented by ensuring that the supply voltage does not drop below the minimum specifications.
- Voltage levels below the minimum recommended voltage level may lead to malfunction. The /Reset pin of the module shall be held on LOW logic level whenever the VCC is not stable or below the minimum operating Voltage.
- Special care must be taken in case of battery powered systems.



- Elements for ESD protection should be placed on all pins that are accessible from the outside and should be placed close to the accessible area. For example, the RF-pin is accessible when using an external antenna and should be protected.
- ESD protection for the antenna connection must be chosen such as to have a minimum effect on the RF signal. For example, a protection diode with low capacitance such as the 8231706A or a 68 nH air-core coil connecting the RF-line to ground give good results.
- Placeholders for optional antenna matching or additional filtering are recommended.
- The antenna path should be kept as short as possible.



Again, no fixed values can be recommended, as they depend on the influencing circumstances of the application (antenna, interferences etc.).





- To avoid the risk of short circuits and interference there should be only the necessary routing underneath the module on the top layer of the baseboard.
- On the second layer, a ground plane is recommended, to provide good grounding and shielding to any following layers and application environment.
- Filter and blocking capacitors should be placed directly in the tracks without stubs, to achieve the best effect.
- Antenna matching elements should be placed close to the antenna / connector, blocking capacitors close to the module.
- Ground connections for the module and the capacitors should be kept as short as possible and with at least one separate through hole connection to the ground layer.
- ESD protection elements should be placed as close as possible to the exposed areas.



7.2 Dimensioning of the micro strip antenna line

The antenna track has to be designed as a 50 Ω feed line. The width W for a micro strip can





be calculated using the following equation:

$$W = 1.25 \times \left(\frac{5.98 \times H}{e^{\frac{50 \times \sqrt{\epsilon_r + 1.41}}{87}}} - T_{met}\right)$$
(1)

Example:

A FR4 material with $\varepsilon_r = 4.3$, a height H = 1000 µm and a copper thickness of T_{met} = 18 µm will lead to a trace width of W ~ 1.9 mm. To ease the calculation of the micro strip line (or e.g. a coplanar) many calculators can be found in the internet.

- As rule of thumb a distance of about 3×W should be observed between the micro strip and other traces / ground.
- The micro strip refers to ground, therefore there has to be the ground plane underneath the trace.
- Keep the feeding line as short as possible.

7.3 Antenna solutions

There exist several kinds of antennas, which are optimized for different needs. Chip antennas are optimized for minimal size requirements but at the expense of range, PCB antennas are optimized for minimal costs, and are generally a compromise between size and range. Both usually fit inside a housing.

Range optimization in general is at the expense of space. Antennas that are bigger in size, so that they would probably not fit in a small housing, are usually equipped with a RF connector. A benefit of this connector may be to use it to lead the RF signal through a metal plate (e.g. metal housing, cabinet).

As a rule of thumb a minimum distance of λ /10 (which is 3.5 cm @ 868 MHz and 1.2 cm @ 2.44 GHz) from the antenna to any other metal should be kept. Metal placed further away will not directly influence the behavior of the antenna, but will anyway produce shadowing.





Keep the antenna as far as possible from large metal objects to avoid electromagnetic field blocking.



The choice of antenna might have influence on the safety requirements.

In the following chapters, some special types of antenna are described.

7.3.1 Wire antenna

An effective antenna is a λ /4 radiator with a suiting ground plane. The simplest realization is a piece of wire. It's length is depending on the used radio frequency, so for example 8.6 cm 868.0 MHz and 3.1 cm for 2.440 GHz as frequency. This radiator needs a ground plane at its feeding point. Ideally, it is placed vertically in the middle of the ground plane. As this is often not possible because of space requirements, a suitable compromise is to bend the wire away from the PCB respective to the ground plane. The λ /4 radiator has approximately 40 Ω input impedance. Therefore, matching is not required.

7.3.2 Chip antenna

There are many chip antennas from various manufacturers. The benefit of a chip antenna is obviously the minimal space required and reasonable costs. However, this is often at the expense of range. For the chip antennas, reference designs should be followed as closely as possible, because only in this constellation can the stated performance be achieved.

7.3.3 PCB antenna

PCB antenna designs can be very different. The special attention can be on the miniaturization or on the performance. The benefits of the PCB antenna are their small / not existing (if PCB space is available) costs, however the evaluation of a PCB antenna holds more risk of failure than the use of a finished antenna. Most PCB antenna designs are a compromise of range and space between chip antennas and connector antennas.



8 Reference design

Adrastea-I was tested on the evaluation board which serves as reference design.

Further information concerning the use of the evaluation board can be found in the manual of the Adrastea-I evaluation board [2].



8.1 Schematic





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User manual Adrastea-I

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User manual Adrastea-I



Figure 25: Circuit diagram 3



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Figure 26: Circuit diagram 4



User manual Adrastea-I



Figure 27: Circuit diagram 5





8.2 Layout





WIRELESS CONNECTIVITY & SENSORS User manual Adrastea-I





Figure 29: Top layer (upper left), second layer (upper right), third layer (bottom left), fourth layer (bottom right)



9 Manufacturing information

9.1 Moisture sensitivity level

This wireless connectivity product is categorized as JEDEC Moisture Sensitivity Level 3 (MSL3), which requires special handling.

More information regarding the MSL requirements can be found in the IPC/JEDEC J-STD-020 standard on *www.jedec.org*.

More information about the handling, picking, shipping and the usage of moisture/reflow and/or process sensitive products can be found in the IPC/JEDEC J-STD-033 standard on *www.jedec.org*.

9.2 Soldering

9.2.1 Reflow soldering

Attention must be paid on the thickness of the solder resist between the host PCB top side and the modules bottom side. Only lead-free assembly is recommended according to JEDEC J-STD020.

Profile feature		Value
Preheat temperature Min	T_{SMin}	150 ℃
Preheat temperature Max	T _{S Max}	200 °C
Preheat time from $T_{S Min}$ to $T_{S Max}$	t _S	60 - 120 seconds
Ramp-up rate (T_L to T_P)		3 ℃ / second max.
Liquidous temperature	TL	217 ℃
Time t_L maintained above T_L	tL	60 - 150 seconds
Peak package body temperature	Τ _Ρ	see table below
Time within 5 $^{ m \circ C}$ of actual peak temperature	t _P	20 - 30 seconds
Ramp-down Rate $(T_P \text{ to } T_L)$		6 ℃ / second max.
Time 20 °C to T _P		8 minutes max.

Table 41: Classification reflow soldering profile, Note: refer to IPC/JEDEC J-STD-020E



Package thickness	Volume mm ³ <350	Volume mm ³ 350-2000	Volume mm ³ >2000
< 1.6 mm	260 ℃	260 ℃	260 °C
1.6 mm - 2.5 mm	260 ℃	250 °C	245 °C
> 2.5 mm	250 °C	245 ℃	245 °C

Table 42: Package classification reflow temperature, PB-free assembly, Note: refer to IPC/-JEDEC J-STD-020E

It is recommended to solder this module on the last reflow cycle of the PCB. For solder paste use a LFM-48W or Indium based SAC 305 alloy (Sn 96.5 / Ag 3.0 / Cu 0.5 / Indium 8.9HF / Type 3 / 89%) type 3 or higher.

The reflow profile must be adjusted based on the thermal mass of the entire populated PCB, heat transfer efficiency of the reflow oven and the specific type of solder paste used. Based on the specific process and PCB layout the optimal soldering profile must be adjusted and verified. Other soldering methods (e.g. vapor phase) have not been verified and have to be validated by the customer at their own risk. Rework is not recommended.







After reflow soldering, visually inspect the board to confirm proper alignment

9.2.2 Cleaning

Do not clean the product. Any residue cannot be easily removed by washing. Use a "no clean" soldering paste and do not clean the board after soldering.

- Do not clean the product with water. Capillary effects can draw water into the gap between the host PCB and the module, absorbing water underneath it. If water is trapped inside, it may short-circuit adjoining pads. The water may also destroy the label and ink-jet printed text on it.
- Cleaning processes using alcohol or other organic solvents may draw solder flux residues into the housing, which won't be detected in a post-wash inspection. The solvent may also destroy the label and ink-jet printed text on it.
- Do not use ultrasonic cleaning as it will permanently damage the part, particularly the crystal oscillators.

9.2.3 Potting and coating

- If the product is potted in the customer application, the potting material might shrink or expand during and after hardening. Shrinking could lead to an incomplete seal, allowing contaminants into the component. Expansion could damage components. We recommend a manual inspection after potting to avoid these effects.
- Conformal coating or potting results in loss of warranty.
- The RF shield will not protect the part from low-viscosity coatings and potting. An undefined amount of coating and potting will enter inside the shielding.
- Conformal coating and potting will influence the parts of the radio front end and consequently influence the radio performance.
- Potting will influence the temperature behaviour of the device. This might be critical for components with high power.

9.2.4 Other notations

- Do not attempt to improve the grounding by forming metal strips directly to the EMI covers or soldering on ground cables, as it may damage the part and will void the warranty.
- Always solder every pad to the host PCB even if some are unused, to improve the mechanical strength of the module.
- The part is sensitive to ultrasonic waves, as such do not use ultrasonic cleaning, welding or other processing. Any ultrasonic processing will void the warranty.



9.3 ESD handling

This product is highly sensitive to electrostatic discharge (ESD). As such, always use proper ESD precautions when handling. Make sure to handle the part properly throughout all stages of production, including on the host PCB where the module is installed. For ESD ratings, refer to the module series' maximum ESD section. For more information, refer to the relevant chapter 2. Failing to follow the aforementioned recommendations can result in severe damage to the part.

- the first contact point when handling the PCB is always between the local GND and the host PCB GND, unless there is a galvanic coupling between the local GND (for example work table) and the host PCB GND.
- Before assembling an antenna patch, connect the grounds.
- While handling the RF pin, avoid contact with any charged capacitors and be careful when contacting any materials that can develop charges (for example coaxial cable with around 50-80 pF/m, patch antenna with around 10 pF, soldering iron etc.)
- Do not touch any exposed area of the antenna to avoid electrostatic discharge. Do not let the antenna area be touched in a non ESD-safe manner.
- When soldering, use an ESD-safe soldering iron.

9.4 Safety recommendations

It is your duty to ensure that the product is allowed to be used in the destination country and within the required environment. Usage of the product can be dangerous and must be tested and verified by the end user. Be especially careful of:

- Use in areas with risk of explosion (for example oil refineries, gas stations).
- Use in areas such as airports, aircraft, hospitals, etc., where the product may interfere with other electronic components.

It is the customer's responsibility to ensure compliance with all applicable legal, regulatory and safety-related requirements as well as applicable environmental regulations. Disassembling the product is not allowed. Evidence of tampering will void the warranty.

- Compliance with the instructions in the product manual is recommended for correct product set-up.
- The product must be provided with a consolidated voltage source. The wiring must meet all applicable fire and security prevention standards.
- Handle with care. Avoid touching the pins as there could be ESD damage.

Be careful when working with any external components. When in doubt consult the technical documentation and relevant standards. Always use an antenna with the proper characteristics.

User manual Adrastea-I





Würth Elektronik eiSos radio modules with high output power of up to 500 mW, as for example the radio module Thebe-II, generate a high amount of warmth while transmitting. The manufacturer of the end device must take care of potentially necessary actions for his application.

10 Physical specifications

10.1 Dimensions

Dimensions		
13.4 * 14.6 * 1.85 mm		

Table 43: Dimensions

Tolerances: see chapter 10.3

10.2 Weight

Weight
0.80 g

Table 44: Weight

Tolerance: \pm 0.15 g





10.3 Module drawing



Figure 31: Module dimensions [mm]



10.4 Footprint







11 Marking

11.1 Lot number

The 15 digit lot number is printed in numerical digits as well as in form of a machine readable bar code. It is divided into 5 blocks as shown in the following picture and can be translated according to the following table.



Figure 33: Lot number structure

Block	Information	Example(s)
1	eiSos internal, 3 digits	439
2	eiSos internal, 2 digits	01
3	Hardware version, 3 digits	V2.4 = 024, V12.2 = 122
4	Date code, 4 digits	1703 = week 03 in year 2017,
		1816 = week 16 in year 2018
5	Firmware version, 3 digits	V3.2 = 302, V5.13 = 513

Table 45: Lot number details

As the user can perform a firmware update the printed lot number only shows the factory delivery state. The currently installed firmware can be requested from the module using the corresponding product specific command. The firmware version as well as the hardware version are restricted to show only major and minor version not the patch identifier.



11.2 General labeling information

The module labels may include the following fields:

- · Manufacturer identification WE, Würth Elektronik or Würth Elektronik eiSos
- WE Order Code and/or article alias
- Serial number or MAC address
- Certification identifiers (CE, FCC ID, IC, TELEC,...)
- Bar code or 2D code containing the serial number or MAC address

If the module is using a Serial Number, this serial number includes the product ID (PID) and an 6 digit number. The 6 rightmost digits represent the 6 digit number, followed by the product ID (2 or 3 digits). Some labels indicate the product ID with a "." as marker in-between the 2 fields. The PID and the 6 digit number form together a unique serial number for any wireless connectivity product.

In case of small labels, the 3 byte manufacturer identifier (0x0018DA) of the MAC address is not printed on the labels. The 3 byte counter printed on the label can be used with this 0018DA to produce the full MAC address by appending the counter after the manufacturer identifier.



Figure 34: Label of the Adrastea-I



12 References

- [1] Würth Elektronik. Adrastea Commander. http://www.we-online.com/ Adrastea-Commander.
- [2] Würth Elektronik. ADRASTEA-I EVALUATION BOARD MANUAL. https://we-online. com/katalog/en/manual/2615029236001.



13 Regulatory compliance information

13.1 Important notice EU

The use of RF frequencies is limited by national regulations. The Adrastea-I has been designed to comply with the RED directive 2014/53/EU of the European Union (EU).

The Adrastea-I can be operated without notification and free of charge in the area of the European Union. However, according to the RED directive, restrictions (e.g. in terms of duty cycle or maximum allowed RF power) may apply.



Since the module is a built-in equipment its power class according to EN 62368-1 must be specified in the end product.

13.2 Conformity assessment of the final product

The Adrastea-I is a subassembly. It is designed to be embedded into other products (products incorporating the Adrastea-I are henceforward referred to as "final products"). It is the responsibility of the manufacturer of the final product to ensure that the final product is in compliance with the essential requirements of the underlying national radio regulations. The conformity assessment of the subassembly Adrastea-I carried out by Würth Elektronik eiSos does not replace the required conformity assessment of the final product.

13.3 Exemption clause

Relevant regulation requirements are subject to change. Würth Elektronik eiSos does not guarantee the accuracy of the before mentioned information. Directives, technical standards, procedural descriptions and the like may be interpreted differently by the national authorities. Equally, the national laws and restrictions may vary with the country. In case of doubt or uncertainty, we recommend that you consult with the authorities or official certification organizations of the relevant countries. Würth Elektronik eiSos is exempt from any responsibilities or liabilities related to regulatory compliance.

Notwithstanding the above, Würth Elektronik eiSos makes no representations and warranties of any kind related to their accuracy, correctness, completeness and/or usability for customer applications. No responsibility is assumed for inaccuracies or incompleteness.



13.4 EU Declaration of conformity



EU DECLARATION OF CONFORMITY

Radio equipment: Adrastea-I

The manufacturer: Würth Elektronik eiSos GmbH & Co. KG Max-Eyth-Straße 1 74638 Waldenburg

This declaration of conformity is issued under the sole responsibility of the manufacturer.

Object of the declaration: Adrastea-I

The object of the declaration described above is in conformity with the relevant Union harmonisation legislation Directive 2014/53/EU and 2011/65/EU with its amending Annex II EU 2015/863. Following harmonised norms or technical specifications have been applied:

> EN 301 908-1 V13.1.1 (2019-11) EN 301 908-13 V13.1.1 (2019-11) EN 303 413 V1.1.1 (2017-06) EN 301 489-1 V2.2.3 (2019-11) EN 301 489-19 V2.1.1 (2019-04) EN 62311: 2008 EN 62368-1: 2014/AC: 2015/A11: 2017

i.A. G. Esclardy

Trier, 14th of February 2022 Place and date of issue



14 Important notes

The following conditions apply to all goods within the wireless connectivity product range of Würth Elektronik eiSos GmbH & Co. KG:

14.1 General customer responsibility

Some goods within the product range of Würth Elektronik eiSos GmbH & Co. KG contain statements regarding general suitability for certain application areas. These statements about suitability are based on our knowledge and experience of typical requirements concerning the areas, serve as general guidance and cannot be estimated as binding statements about the suitability for a customer application. The responsibility for the applicability and use in a particular customer design is always solely within the authority of the customer. Due to this fact, it is up to the customer to evaluate, where appropriate to investigate and to decide whether the device with the specific product characteristics described in the product specification is valid and suitable for the respective customer application or not. Accordingly, the customer is cautioned to verify that the documentation is current before placing orders.

14.2 Customer responsibility related to specific, in particular safety-relevant applications

It has to be clearly pointed out that the possibility of a malfunction of electronic components or failure before the end of the usual lifetime cannot be completely eliminated in the current state of the art, even if the products are operated within the range of the specifications. The same statement is valid for all software sourcecode and firmware parts contained in or used with or for products in the wireless connectivity and sensor product range of Würth Elektronik eiSos GmbH & Co. KG. In certain customer applications requiring a high level of safety and especially in customer applications in which the malfunction or failure of an electronic component could endanger human life or health, it must be ensured by most advanced technological aid of suitable design of the customer application that no injury or damage is caused to third parties in the event of malfunction or failure of an electronic.

14.3 Best care and attention

Any product-specific data sheets, manuals, application notes, PCN's, warnings and cautions must be strictly observed in the most recent versions and matching to the products firmware revisions. This documents can be downloaded from the product specific sections on the wireless connectivity homepage.

14.4 Customer support for product specifications

Some products within the product range may contain substances, which are subject to restrictions in certain jurisdictions in order to serve specific technical requirements. Necessary information is available on request. In this case, the field sales engineer or the internal sales person in charge should be contacted who will be happy to support in this matter.



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Due to constant product improvement, product specifications may change from time to time. As a standard reporting procedure of the Product Change Notification (PCN) according to the JEDEC-Standard, we inform about major changes. In case of further queries regarding the PC-N, the field sales engineer, the internal sales person or the technical support team in charge should be contacted. The basic responsibility of the customer as per section 14.1 and 14.2 remains unaffected. All wireless connectivity module driver software "wireless connectivity SDK" and it's source codes as well as all PC software tools are not subject to the Product Change Notification information process.

14.6 Product life cycle

Due to technical progress and economical evaluation we also reserve the right to discontinue production and delivery of products. As a standard reporting procedure of the Product Termination Notification (PTN) according to the JEDEC-Standard we will inform at an early stage about inevitable product discontinuance. According to this, we cannot ensure that all products within our product range will always be available. Therefore, it needs to be verified with the field sales engineer or the internal sales person in charge about the current product availability expectancy before or when the product for application design-in disposal is considered. The approach named above does not apply in the case of individual agreements deviating from the foregoing for customer-specific products.

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The incorporated firmware created by Würth Elektronik eiSos is and will remain the exclusive property of Würth Elektronik eiSos.

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You have the opportunity to request the current and actual firmware for a bought wireless connectivity product within the time of warranty. However, Würth Elektronik eiSos has no obligation to update a modules firmware in their production facilities, but can offer this as a service on request. The upload of firmware updates falls within your responsibility, e.g. via ACC or another software for firmware updates. Firmware updates will not be communicated automatically. It is within your responsibility to check the current version of a firmware in the latest version of the product manual on our website. The revision table in the product manual provides all necessary information about firmware updates. There is no right to be provided with binary files, so called "firmware images", those could be flashed through JTAG, SWD, Spi-Bi-Wire, SPI or similar interfaces.

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We recommend you to be updated about the status of new firmware and software, which is available on our website or in our data sheet and manual, and to implement new software in your device where appropriate.

By ordering a product, you accept these license terms in all terms.



List of Figures

1	Adrastea-I
2	Adrastea-I GCF Certification
3	Adrastea-I Deutsche Telekom Certification
4	Normal Cellular Certification Process
5	Benefits of Deutsche Telekom Certified Module
6	Block diagram
7	Pinout (top view)
8	Adrastea-I Power up Sequence
9	UART0 Host Interface
10	SPIM Connection
11	I ² C Connection
12	Adrastea-I State Transition
13	Adrastea-I: Sony MCU portal registration
14	Adrastea-I: Sony MCU portal Access
15	Minimal pin connections
16	Adrastea Commander
17	Adrastea Commander
18	COM ports detected - Adrastea commander
19	MiniConsole start view - Adrastea Commander
20	SIM card detected - Adrastea Commander
21	Lavout
22	Dimensioning the antenna feed line as micro strip
23	Circuit diagram 1
24	Circuit diagram 2
25	Circuit diagram 3
26	Circuit diagram 4
27	Circuit diagram 5
28	Assembly diagram 74
29	Top laver (upper left) second laver (upper right) third laver (bottom left) fourth
20	laver (bottom right)
30	Beflow soldering profile 77
31	Module dimensions [mm]
30	Footprint and dimensions [mm]
33	$1 \text{ or prime and dimensions [mm]} \dots \dots$
24	
34	Laber UI lite Aurastea-1

List of Tables

1	Module Key Features
2	Ordering information
3	Recommended operating conditions
4	LTE-Cat.M Current consumption
5	NB-IoT Current consumption
6	LTE-Cat.M Supported Bands
7	LTE-Cat.NB-IoT Supported Bands

User manual Adrastea-I



8	LTE-Cat.M RX Sensitivity	19
9	LTE-Cat.NB-IoT RX Sensitivity	19
10	LTE-Cat.M Maximum Output Power	20
11	LTE-Cat.NB-IoT Maximum Output Power	20
12	Radio characteristics	21
13	GNSS RX Sensitivity	22
14	GNSS Time to First Fix	22
15	GNSS Position Accuracy	22
16	Pinout	24
17	Pinout1	25
18	Pinout2	26
19	Pinout3	27
20	Pinout4	28
21	Power Up timing	28
22	EXT ALARM Pin	31
23	E-JTAG Debug port	33
24	GPIO Pin Information	34
25	Digital IO Pins Specifications	34
26	UART Interfaces	35
27	UART Default Configuration	35
28	UARTO Pin Interface	36
29	UART1 Pin Interface	36
30	UART2 Pin Interface	37
31	SPIM Pin Interface	39
32	I ² C Pin Interface	41
33	ADC Interfaces	43
34	ADC Functional Specifications	43
35	Measured Input Resistance	44
36	ADC Pin Interface	44
37	SIM Pin Interface	44
38	RF Pin Interface	45
39	E-JTAG Debug port	45
40	GPIO Pin Information	46
41	Classification reflow soldering profile, Note: refer to IPC/JEDEC J-STD-020E	76
42	Package classification reflow temperature, PB-free assembly, Note: refer to IPC/-	
	JEDEČ J-STD-020E	77
43	Dimensions	81
44	Weight	81
45	Lot number details	84



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